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*FG-ANX201: Using Xtium-CL MX4 and Xtium2-CL MX4 Appnote*

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## Using Xtium2-CL MX4 and Xtium-CL MX4 interchangeably

### **Overview**

Teledyne DALSA has designed the Xtium2-CL MX4 frame grabber to ease the supply chain issue facing the Xtium-CL MX4. The Xtium2-CL MX4 supports the same feature set and therefore maintains full compatibility with the Xtium-CL MX4. As a result, users can easily adapt their current systems to work with either board.

This application note targets the current users of Xtium-CL MX4 and describes how to make an application support both boards.

### **Prerequisites**

- An application developed using an Xtium-CL MX4 frame grabber.
- An installed Xtium2-CL MX4 frame grabber.

**IMPORTANT NOTE: Teledyne DALSA will continue supplying both Xtium2-CL MX4 and Xtium-CL MX4 for a foreseeable future.**

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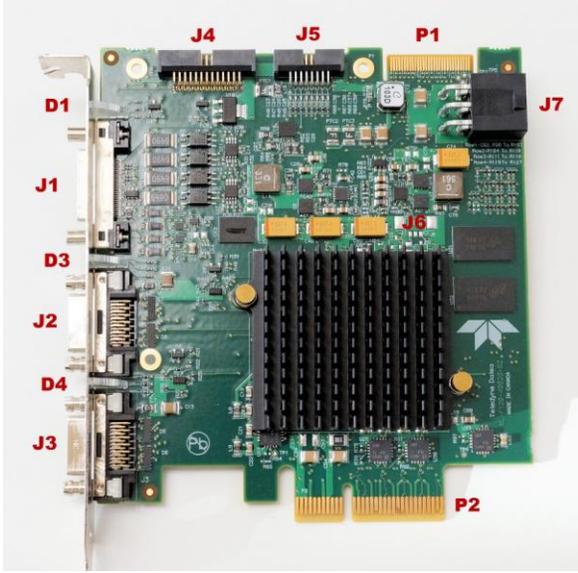
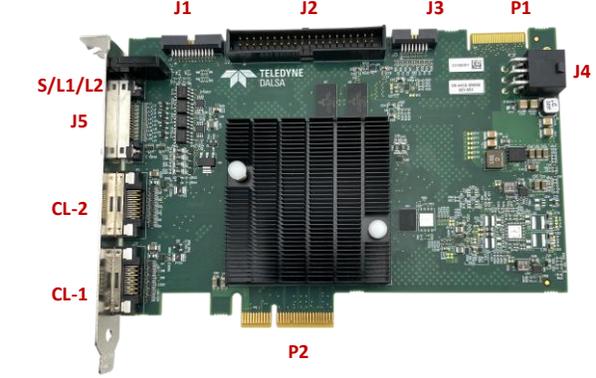
## What's new in Xtium2-CL MX4

Although the Xtium2-CL MX4 supports all the features of Xtium-CL MX4, we have taken advantage of the new design cycle to add a few new features to the Xtium2-CL MX4 board:

- **PCIe Gen 3 Readiness:** The Xtium2-CL MX4 is PCI Express Gen 3 ready. The PCIe Gen 3 is fully backward compatible with PCIe Gen 2 used on the Xtium-CL MX4.
- **The General Purpose I/O:** The Xtium2-CL MX4 general purpose I/O signal and connectors are fully compatible with those of the Xtium-CL MX4. All cables designed for the Xtium-CL MX4 can be used with Xtium2-CL MX4 without change. In addition to the I/O connectors found on the Xtium-CL MX4, the Xtium2-CL MX4 also features a 20X2 100<sup>TH</sup> 40-pin connector, which can be used with the DB37 bracket assembly (part number: OR-X4CC-IOCAB).

# Boards' PCB and Bracket

The table below depicts the boards and brackets of the Xtium-CL MX4 and Xtium2-CL MX4.

<p><b><i>Xtium-CL MX4</i></b></p> 	<p><b><i>Xtium2-CL MX4</i></b></p> 
<p><b><i>Xtium-CL MX4 Bracket</i></b></p> 	<p><b><i>Xtium2-CL MX4 Bracket</i></b></p> 

**Additional notes:**

- The Xtium2-CL MX4 requires 3.3 V from the PCI slot to provide a minimum of 4.5 W; the Xtium-CL MX4 generates 3.3 V from PCI 12 V and so does not use the 3.3 V from the slot.
- At power up, the Xtium2-CL MX4 status LED starts blue before turning green on driver start up; for the for the Xtium-CL MX4, the LED is green.

## PCB Connector Levels

The following table lists the Xtium-CL-MX4 connectors and their counterpart in the Xtium2-CL MX4.

Feature	Xtium-CL MX4	Xtium2-CL MX4
Camera Link Input #1	CL-1 (J3)	CL-1
Camera Link Input #2	CL-2 (J2)	CL-2
External Signals connector DH60-27P	J1	J5
LEDs	D1/D3/D4	S/L1/L2
Internal I/O Signals connector (26-pin SHF-113-01-L-D-RA)	J4	J1
Multi Board Sync	J5	J3
PC power for PoCL	J7	J4
PCIe [P2]	Gen2 x4 Max bandwidth to host: 1.7 GB/s	Gen3 x4 Max bandwidth to host: 3.4 GB/s
Internal I/O Signals connector (40-pin TST-120-01-G-D)	-	J2

## Compatibility and Compliance

Attribute	Details	Notes
<b>Feature support</b>	See Table 1 in the appendix for details	
<b>Sapera LT SDK</b>	Version 8.20 or higher	
<b>Input camera formats</b>	See Table 2 in the appendix for details	
<b>Window 10/Windows 11</b>	32-bit/64-bit, Wow64	Device driver versions: 1.x or higher
<b>Windows 7/Windows 8</b>	32-bit/64-bit, Wow64	Device driver versions: 1.00.00.0023 or lower
<b>Linux</b>	Kernel 5.15	Device driver version 1.01
<b>Compliance</b>	FCC Class A CE, UKAC ROHS, China RoHS, South Korea KC	

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# How to make existing applications work with Xtium2-CL MX4

A board device driver allows a Sopera LT-based user application to control and capture images from a frame grabber. The Xtium2-CL MX4 and Xtium-CL MX4 boards have their own specific device drivers. Multiple device drivers can co-exist in a system. A device driver is functional only if a corresponding board is present in the computer at power up.

There are two different ways to adapt your system to the Xtium2-CL MX4:

- Changing your application to use Xtium2-CL MX4 as a new board.
- Using Xtium2-CL MX4 without changing your application.

Let's see how each of these options can be achieved.

## 1. Changing user application to use Xtium2-CL MX4

The Teledyne DALSA Sopera LT API is hardware agnostic and allows an existing application to support new Teledyne DALSA image acquisition devices such as Xtium2-CL MX4 with minimal changes. The Sopera LT API uses the concept of an acquisition server to represent an acquisition device. The device driver for the specific hardware acquisition device contains the name of the server, which the application uses to communicate with the device.

To use either the Xtium-CL MX4 or Xtium2-CL MX4 board in a system, modify the application code to look for the Xtium2-CL MX4 server name. Here is a code snippet that accomplishes this:

```
const char serverName1[CORSERVER_MAX_STRLEN] = "Xtium-CL_MX4_1";
const char serverName2[CORSERVER_MAX_STRLEN] = "Xtium2-CL_MX4_1";
CORSERVER server_MX4 = NULL;
If( !SapManager::GetServerHandle(serverName1, &server_MX4))
{
    If (!SapManager::GetServerHandle(serverName2, &server_MX4))
    {Error...}
}
```

The above example describes a simple case where only one board per system is used at a time. Of course, there are several other ways in which support for new Teledyne DALSA acquisition devices can be added to the user applications; refer to the Sopera LT SDK documentation and accompanying examples for additional details.

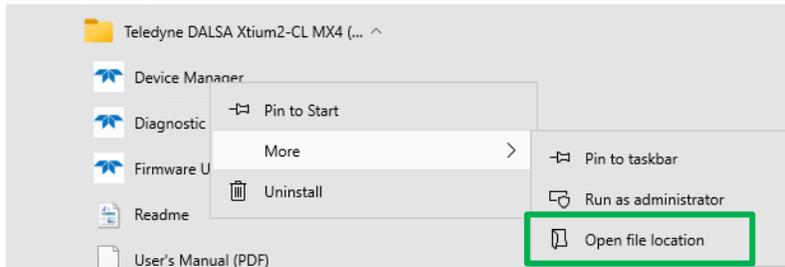
## 2. Using Xtium2-CL MX4 without changing the application code

The Xtium2-CL MX4 device driver allows users to mimic the Xtium-CL MX4 server name. This allows applications to use the new board without change or recompilation. The limitation in this approach is that Xtium-CL MX4 and Xtium2-CL MX4 boards cannot co-exist in the same system.

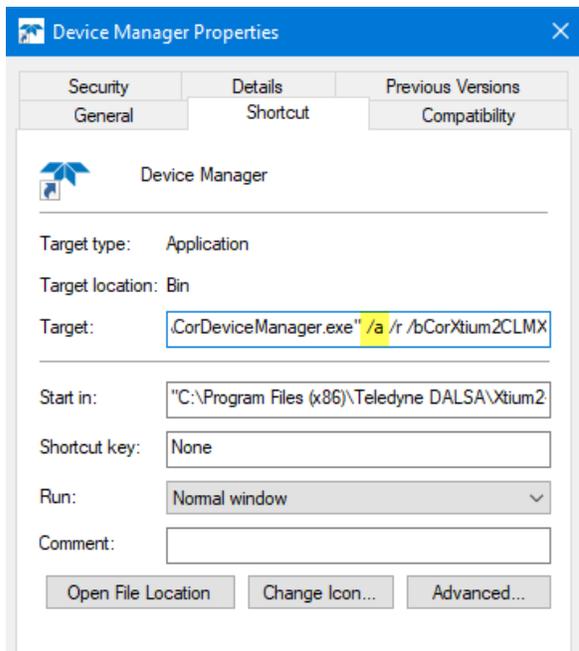
Here are the steps to change Xtium2-CL MX4 server name to Xtium-CL MX4 server name.  
**Note, this procedure requires administrator rights to your system.**

### To change the frame grabber ServerName

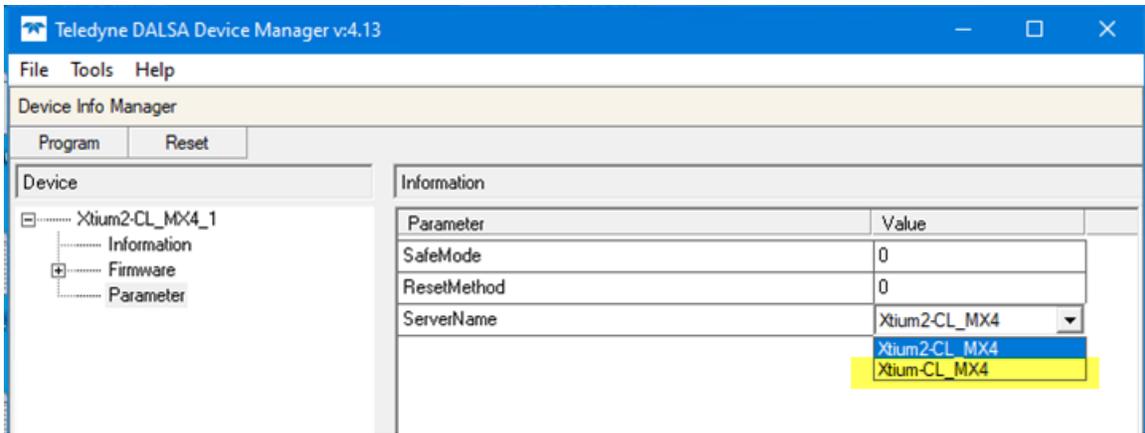
1. On the **Start** menu, open the **Teledyne DALSA Xtium2-CL MX4** folder.
2. On the shortcut menu of the **Device Manager**, select **More > Open file location**.



3. On the shortcut menu of the Device Manager, select **Properties**.
4. In the **Target** box, add the following option to the command line, as highlighted: `/a`. Click **OK**.



5. On the shortcut menu of the Device Manager, select **Run as administrator**.
6. Expand the Xtium2-CL\_MX4\_1 node and select **Parameter**.
7. Change ServerName from Xtium2-CL\_MX4 to Xtium-CL\_MX4.



8. Click **Program** and then **Reset** to make it effective.

# Appendix: Xtium-CL MX4 and Xtium2-CL MX4 Feature and Tap Configuration Comparison

The following two tables provide a comparison between the two frame grabbers regarding supported features and tap configurations.

Table 1. Supported features.

Features	Xtium-CL MX4	Xtium2-CL MX4
Host Bus	PCI Express Rev. 2.0	PCI Express 3.0
Bus slot	x4	x4
Host Bus Compatibility	PCIe Gen 1	PCIe Gen 2/1
Host Bandwidth:	x	x
PCIe x4 Gen3	1750MB/s	<b>3400MB/s</b>
PCIe x4 Gen2	1750MB/s	1750MB/s
PCIe x4 Gen1	850MB/s	850MB/s
Area Scan Cameras – Mono, Color: RGB & Bayer	x	x
Line Scan Cameras – Mono, Color: RGB, RGB Packed & Bicolor	x	x
Segmented taps (e.g., support for cameras like Teledyne DALSA HS 8K, P3 12K): Supports 2, 4, 8 “alternate” taps; all directions	x	x
Dual Base configurations on single board	x	x
J4 Connector	x	x
Monochrome camera support:	(P=Parallel taps; S=Segmented Taps)	
Supports 2x CameraLink Base		
8-bits/pixel: 1, 2, 3-taps	P,S	P,S
10/12-bits/pixel: 1, 2-taps	P,S	P,S
14/16-bits/pixel: 1-tap		
Supports CameraLink Medium, Full modes		
Supports 1x CameraLink Medium or Full		
8-bits/pixel: 1, 2, 3, 4, 6, 8-taps	P,S	P,S
8/10/12-bits/pixel: 1, 2, 4, 6-taps	P,S	P,S
Supports CameraLink 80-bit		
8-bits/10-taps	P	P
10bits/8-taps	P	P
Standard CameraLink Configurations:		
Base: RGB 1T8B (1-tap 8-Bit/pixel/color)	x	x
Medium: RGB 2T8B, 1T10B, 1T12B	x	x
Extended configurations:		
80-Bit (DECA): RGB 10T8B	x	x
80-Bit (DECA): RGB 8T8B	x	x
Line scan Bi-color modes 80-Bit: RGBG 10T8B	x	x
White Balance	x	x
Lookup Tables	x	x
Pixel Clock Input: 85MHz Max.	x	x
Connectors		
Camera Link	2xSDR	2xSDR
General purpose I/O(main bracket)	DH60	DH60
General purpose I/O(Aux#1)	26-pin,0.05"	26-pin,0.05"
General purpose I/O(Aux#2)	N/A	40-pin,0.1"
Multi-Board sync	16-pin,0.05"	16-pin,0.05"
Auxiliar Power for (PoCL)	ATX 6-pin (male)	ATX 6-pin (male)
Board size (PCIe Half-Length)	4x4.2in/10cmx10.7cm	4x6.4in/10cmx16.3cm
On-board memory	512MB	<b>1GB</b>
PoCL: Base/Medium/Full (2x4W max.)	x	x
Cable Length: 10 meters at 85MHz	x	x
Multi-Board sync	x	x
Status/Diagnostic LEDs to indicate:	x	x
PCIe link capability Gen1/Gen2/Gen3	x	x
Board status	x	x
Camera connection status	x	x
Grab status	x	x
Operations Systems: Microsoft® Windows® 10, Windows 7, Windows 8/8.1 32/64 and WOW64	x	x

Table 2. Supported tap configurations.

Supported Tap Configurations									
Firmware	Module	Area-scan	Line-scan	Sapera Equivalent	Supported Bits Per Pixel	Taps	Xtium-CL MX4	Xtium2-CL MX4	
1 x Full Camera Link	CameraLink Full Mono CameraLink Full Bayer	1X-1Y	1X	One Tap Left to Right	8, 10, 12, 14, 16	1	x	x	
		1X-2Y	2X-2Y	One Tap Left to Right 2 channels	8, 10, 12,14, 16	2	x	x	
		1X2-1Y	1X2	Two Taps Interleaved (Parallel)	8, 10, 12	2	x	x	
		1X2-2Y	1X2-2Y	Two Taps Interleaved (Parallel) 2 channels	8, 10, 12	4	x	x	
		2X-1Y	2X	Two Taps Separate (Segmented)	8, 10, 12, 14	2	x	x	
		2X-2Y	2X-2Y	Two Taps Separate (Segmented) 2 channels	8, 10, 12, 14	4	x	x	
		2XE-1Y	2XE			2	x	x	
		2XM-1Y	2XM			2	x	x	
		1X3-1Y	1X3	Three Taps Interleaved (Parallel)	8, 10, 12	3	x	x	
		3X-1Y	3X	Three Taps Separate (Segmented)	8, 10, 12	3	x	x	
		1X4-1Y	1X4	Four Taps Interleaved (Parallel)	8, 10, 12	4	x	x	
		1X4-2Y	1X4-2Y	Four Taps Interleaved (Parallel) 2 channels	8	8	x	x	
		4X-1Y	4X	Four Taps Separate (Segmented)	8, 10, 12	4	x	x	
		4X-2Y	4X-2Y	Four Taps Separate (Segmented) 2 channels	8	8	x	x	
		2X2-1Y	2X2	Four Taps Two Segments Interleaved	8, 10, 12	4	x	x	
		2X2-2Y	2X2-2Y	Four Taps Two Segments Interleaved 2 channels	8	8	x	x	
		2X2E-1Y	2X2E	Four Taps Interleaved Converge	8, 10, 12	4	x	x	
		2X2E-2Y	2X2E-2Y	Four Taps Interleaved Converge 2 channels	8	8	x	x	
		1X8-1Y	1X8	Eight Taps Interleaved	8	8	x	x	
		8X-1Y	8X	Eight Taps Separate (Parallel)	8	8	x	x	
	4X2-1Y	4X2			8	x	x		
	4X2E-1Y	4X2E			8	x	x		
	CameraLink Medium Color RGB	1X-1Y	1X	One Tap Left to Right	8, 10, 12	1	x	x	
		1X2-1Y	1X2	Two Taps Interleaved (Parallel)	8	2	x	x	
		2X-1Y	2X	Two Taps Separate (Segmented)	8	2	x	x	
		2XE-1Y	2XE			2	x	x	
		2XM-1Y	2XM			2	x	x	
	CameraLink Full Packed RGB	1X-1Y	1X	One Tap Left to Right	8	1	x	x	
	2 x Base Camera Link	CameraLink Base Mono #1/#2 CameraLink Base Bayer #1/#2	1X-1Y	1X	One Tap Left to Right	8, 10, 12, 14, 16	1	x	x
			1X-2Y	1X-2Y	One Tap Left to Right	8, 10,12	2	x	x
1X2-1Y			1X2	Two Taps Interleaved (Parallel)	8, 10, 12	2	x	X	
2X-1Y			2X	Two Taps Separate (Segmented)	8, 10, 12	2	x	x	
2XE-1Y			2XE			2	x	x	
2XM-1Y			2XM			2	x	x	
1X3-1Y		1X3	Three Taps Interleaved (Parallel)	8	3	x	x		
3X-1Y		3X	Three Taps Separate (Segmented)	8	3	x	x		
CameraLink Base Color RGB #1/#2	1X-1Y	1X	One Tap Left to Right	8	1	x	x		
80-Bits Camera Link	CameraLink 10-Tap/8-Bit Mono	1X10-1Y	1X10	Ten Taps Interleaved (Parallel)	8	10	x	x	
	CameraLink 8-Tap/10-Bit Mono	1X8-1Y	1X8	Eight Taps Interleaved (Parallel)	10	8	x	x	
	CameraLink 80-bit Packed/8-Bit RGB	1X-1Y	1X	One Tap Left to Right	8	1	x	x	
	CameraLink 80-bit Packed/8-Bit Bi-Color	1X-1Y	1X	One Tap Left to Right	8	1	x	x	
	CameraLink 10-Tap/8-Bit Bayer	1X10-1Y	1X10	Ten Taps Interleaved (Parallel)	8	10	x	x	
	CameraLink 8-Tap/10-Bit Bayer	1X8-1Y	1X8	Eight Taps Interleaved (Parallel)	10	8	x	x	